Claim Amendments

Please amend claims 1-5, 21-30 as follows:

Please cancel claims 6-20, and 31-39 as follows:

Please add new claims 40-53 as follows:

Listing of Claims

1. (currently amended) A [[a]] semiconductor device comprising:

a substrate having a surface orientation of (100);

a gate electrode formed on the substrate;

[[a]] Slim spacers formed on the top of the substrate adjacent the gate electrode, said Slim spacers thinned to expose portions of an underlying source drain extension regions (SDE);

wherein source/drain regions are oriented having a source-to-drain axis ~~is formed~~ along the <100> direction.

2. (currently amended) The semiconductor device of claim 1, wherein the width of the Slim spacers is less than about 500 Angstroms.

3. (currently amended) The semiconductor device of claim 1, wherein the ~~polysilicon~~ gate electrode comprises a gate structure ~~comprises~~ having a gate length of less than about 80 nanometers.

4. (currently amended) The semiconductor device of claim 1, ~~forming~~

further comprising at least one ~~dielectric layer~~ tensile-stress film over the ~~polysilicon~~ gate ~~structure~~ electrode and Slim spacers ~~in tensile stress~~.

5. (currently amended) The semiconductor device of claim 4, wherein the tensile-stress film exerts a tensile stress [[of]] at a magnitude of about 50 MPa to about 2 GPa.

Claims 6-20 cancelled

21. (currently amended) A CMOS structure having a reduced S/D electrical resistance and increased charge carrier mobility in a channel region comprising:

a semiconductor substrate;

a gate structure formed overlying the semiconductor substrate comprising a ~~polysilicon~~ gate electrode;

thinned spacers adjacent either side of the ~~polysilicon~~ electrode comprising an oxide/nitride portion adjacent the ~~polysilicon~~ electrode;

wherein the width of said thinned spacers is adjusted to control a subsequent stress exerted on a channel region underlying the gate electrode;

wherein said thinned spacers have a top portion at about the same level as the top portion of the gate electrode;

~~and,~~ wherein source/drain extension (SDE) regions comprising the semiconductor substrate extend beyond a maximum width of the spacers; and,

at least one stressed dielectric layer disposed overlying the gate structure including said thinned spacers to exert a stress through said thinned spacers on said channel region.

22. (currently amended) The CMOS structure of claim 21 [[25]], ~~further comprising~~ wherein the at least one stressed dielectric layer is in one of tensile and compressive stress ~~overlying the gate structure and spacers~~.

23. (currently amended) The CMOS structure of claim 21 [[26]], wherein the at least one stressed dielectric layer is selected from the group

consisting of silicon oxide, silicon nitride, silicon oxynitride, silicon carbide, and silicon oxycarbide.

24. (currently amended) The CMOS structure of claim 21 [[25]], further comprising salicide portions comprising a portion of the SDE doped regions.

25. (currently amended) The CMOS structure of claim 21 [[25]], wherein the gate structure gate length is less than about 80 nm.

26. (currently amended) The CMOS structure of claim 21 [[25]], wherein the maximum width of the thinned spacers is less than about 500 Angstroms.

27. (currently amended) The CMOS structure of claim 21 [[25]], wherein the maximum width of the thinned spacers is less than about 400 Angstroms.

28. (currently amended) The CMOS structure of claim 21 [[25]], wherein the oxide portion comprises CVD silicon oxide.

29. (currently amended) The CMOS structure of claim 21 [[25]], wherein the nitride portion is selected from the group consisting of CVD

silicon nitride and CVD silicon oxynitride.

30. (currently amended) The CMOS structure of claim 21 [[25]], wherein the thinned spacers comprises substantially vertical sidewalls.

claims 31-39 cancelled.

40. (new) The semiconductor device of claim 1, wherein the gate electrode comprises a PMOS device.

41. (new) The semiconductor device of claim 1, wherein the Slim spacers have a width that is less than the width of the SDE regions by greater than about 20 percent.

42. (new) The semiconductor device of claim 1, further comprising salicide portions on the SDE regions.

43. (new) The semiconductor device of claim 4, wherein the tensile-stress film is selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, silicon carbide, and silicon oxycarbide.

44. (new) The CMOS structure of claim 21, wherein the gate structure

comprises a PMOS device and the stressed dielectric layer in tensile stress.

45. (new) The CMOS structure of claim 21, further comprising source/drain regions oriented having a source-to-drain axis along the <100> direction.

46. (new) The CMOS structure of claim 21, wherein the thinned spacers have a width that is less than the width of the SDE regions by greater than about 20 percent.

47. (new) A semiconductor device comprising:

a substrate having a surface orientation of (100);

a gate electrode formed on the substrate;

Slim spacers formed on the top of the substrate adjacent either side of the gate electrode, said Slim spacers thinned to control a channel stress;

wherein source/drain regions are oriented having a source-to-drain axis along the <100> direction.

48. (new) The semiconductor device of claim 47, wherein the width of the Slim spacers is less than about 500 Angstroms.

49. (new) The semiconductor device of claim 47, wherein the gate electrode comprises a gate structure having a gate length of less than about 80 nanometers.

50. (new) The semiconductor device of claim 47, further comprising at least one dielectric tensile-stress film over the gate electrode and spacers.

51. (new) The semiconductor device of claim 50, wherein the tensile-stress film exerts a tensile stress at a magnitude of about 50 MPa to about 2 GPa.

52. (new) The semiconductor device of claim 47, wherein said slim spacers have a top portion at about the same level as the top portion of the gate electrode.

53. (new) The semiconductor device of claim 47, wherein the top portion of the Slim spacers is at about the same level as the top portion of the gate electrode.